P/Active™ IEEE 1284 ECP/EPP Termination Network

Features

- Single chip IEEE 1284 parallel port termination
- 28 pin QSOP package, smallest physical solution
- 17 terminating lines in a single package
- In system ESD protection to 8KV, HBM
- In system ESD protection to 4KV per IEC1000-4-2
- Protects downstream devices to 30V

Applications

- ECP/EPP Parallel Port termination
- PC Peripherals
- Notebook and Desktop computers
- Engineering Workstations and Servers

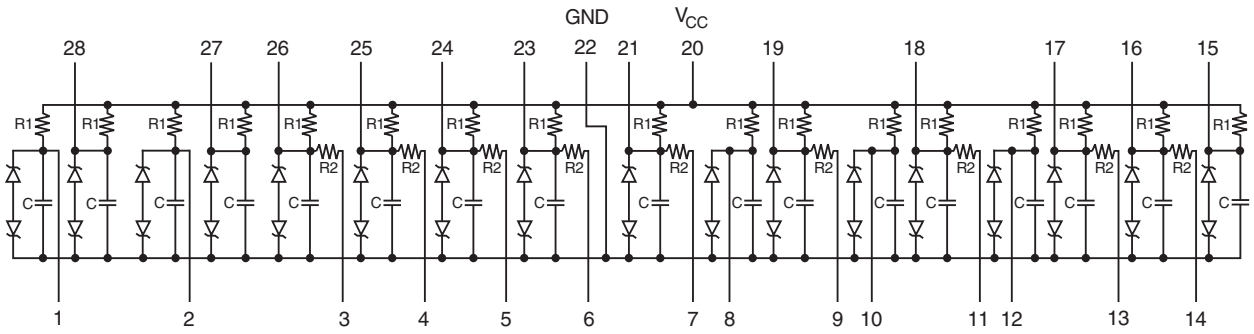
Product Description

California Micro Devices' PACS1284 Parallel Port Termination Network provides a complete integrated solution for the entire IEEE 1284 interface in a single QSOP package.

Advanced, enhanced high-speed parallel ports, conforming to the IEEE 1284 standard, are used to provide communications with external devices such as tape back-up drives, ZIP drives, printers, parallel port SCSI adapters, external LAN adapters, scanners, video capture, and other PC peripherals. These advanced ports support bi-directional transfers to 2MB/sec. To effectively support these higher transfer data rates, the IEEE 1284 standard recommends a combined termination, pull-up filter network between the driver/receiver and the cable at both ends of the parallel port interface. In addition, government EMC compatibility requirements impose strict filtering on the parallel port. California Micro Devices' PACS1284 Parallel Port Termination Network addresses all of these requirements by providing a seventeen line, IEEE 1284 compliant network in a thin film integrated circuit. The device provides a complete parallel port termination solution for space critical applications by integrating a total of 43 discrete components. In addition, all I/O pins are ESD protected for contact discharges up to 4KV per the Human Body Model. However, the output pins of the device which have the highest probability of exposure to ESD pulses are protected to 8KV, HBM, thereby providing the necessary robustness for the port's application environment.

California Micro Devices' P/Active technology provides high reliability and low cost through manufacturing efficiency. The resistors and capacitors are fabricated using proprietary state-of-the-art thin film technology. California Micro Devices' solution is silicon-based and has the same reliability characteristics as today's integrated circuits.

SCHEMATIC CONFIGURATION



STANDARD PART ORDERING INFORMATION

	Package		Ordering Part Number		
RC Code	Pins	Style	Tubes	Tape & Reel	Part Marking
02	28	QSOP	PACS1284-02Q/T	PACS1284-02Q/R	PACS128402Q
04	28	QSOP	PACS1284-04Q/T	PACS1284-04Q/R	PACS128404Q

C1420800

STANDARD SPECIFICATIONS	
Absolute Tolerance (R)	±10%
Absolute Tolerance (C)	±20%
Operating Temperature Range	0°C to 70°C
V_{CC}	6V Max
Power Rating/Resistor	100mW
Maximum Leakage Current (at V_{CC} Max)	1µA@25°C
Signal Clamp Voltage: Positive Clamp Negative Clamp	 >6V <–6V
Storage Temperature	–65°C to 150°C
Package Power Rating	1.00W, Max

STANDARD VALUES			
R1(Ω)	**R2(Ω)**	**c(pF)**	**RC Code**
2.2K	33	220	02
4.7K	33	180	04

ESD SPECIFICATIONS		
ESD Protection*	**Min**	**Max**
Peak Discharge Voltage at any I/O, Human Body Model, Method 3015 (Note 1)	–4KV	4KV
In System Protection, HBM (Note 2)	–8KV	8KV
In System Protection, IEC 1000-4-2, Level 2 (Note 1, 2)	–4KV	4KV
Channel Clamp Voltage @ 8KV ESD Pulses, HBM (Note 1, 2)	–30V	30V

* Guaranteed by design

Note 1: Human Body Model per MIL-STD-883, Method 3015
$C_{Discharge}$ = 100pF, $R_{Discharge}$ = 1.5 KΩ, pin 20 @ 5V and pin 22 @ ground.
ESD Contact Discharge from I/O pins 1, 2, 8, 10, 12, 15, 16, 17, 18, 19, 21, 23 through 28 to ground (pin22), one at a time.

Note 2: Pin 22 grounded, pin 20 to V_{CC}, all other pins are open. ESD contact discharge between ground and pins 1, 2, 8, 10, 12, 15, 16, 17, 18, 19, 21, 23 through 28, one at a time.

Note 3: Standard IEC 1000-4-2 with $C_{Discharge}$ = 150pF, $R_{Discharge}$ = 330Ω, pin 20 @ 5V and pin 22 @ ground.

Application Information

The IEEE 1284 specification requires both termination and EMI filtering on a total of 17 signal lines. Control and Status lines (8 in total) only require a pull-up resistor and a filter capacitor. The Data lines and Strobe also require a series termination resistor in addition to the pull resistors and filter capacitors. See Table 1 and Schematic Diagram.

Signal Name	Series Termination
Data1 - Data8	Yes
Strobe	Yes
Init	Not Required
AutoFeedXT	Not Required
Selectin	Not Required
Ack	Not Required
Busy	Not Required
Paper Empty	Not Required
Select	Not Required
Fault	Not Required

Table 1.

IEEE 1284 defines three interface connectors:

- 1284-A is a 25-pin DB series connector which is the defacto PC standard for the host connection.
- 1284-B is a 36-pin, 0.085 inch centerline connector used on the peripheral device.
- 1284-C is a new 36-pin, 0.050 inch centerline connector which can be used for both host and peripheral.

Figure 1 shows a possible hook-up between the 1284-A connector on a PC motherboard and the PACS1284, illustrating how the pin configuration of the PACS1284 allows for easy interconnects between the two. The dotted I/O signals of the PACS1284 will typically be connected to a Super I/O chip on the motherboard.

Figure 2 shows a possible hook-up between the 1284-B connector on a peripheral and the PACS1284.

Figure 3 shows a possible hook-up between the 1284-C connector and the PACS1284.

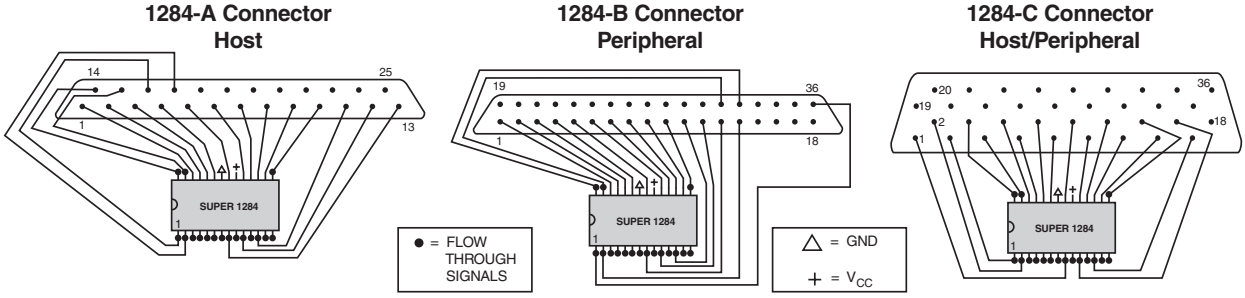


Figure 1. **Figure 2.** **Figure 3.**

Sample Hook-ups of IEEE 1284 Connectors and PACS1284.
(connector and PACS1284 not drawn to scale)

Table 2 defines the signals for the three connectors.

IEEE 1284 Connector Pinouts			
Pin Number	**1284-A 25-pin Dsub**	**1284-B 36-pin Champ**	**1284-BC 36-pin high density**
1	STROBE	STROBE	BUSY
2	Data1	Data1	Select
3	Data2	Data2	ACK
4	Data3	Data3	FAULT
5	Data4	Data4	PError
6	Data5	Data5	Data1
7	Data6	Data6	Data2
8	Data7	Data7	Data3
9	Data8	Data8	Data4
10	ACK	ACK	Data5
11	BUSY	BUSY	Data6
12	PError	PError	Data7
13	Select	Select	Data8
14	AUTOFD	AUTOFD	INIT
15	FAULT	Not Defined	STROBE
16	INIT	Logic Ground	Selectin
17	Selectin	Chassis Ground	AUTOFD
18	Ground	Peripheral Logic High	Host Logic High
19	Ground	Ground	Ground
20	Ground	Ground	Ground
21	Ground	Ground	Ground
22	Ground	Ground	Ground
23	Ground	Ground	Ground
24	Ground	Ground	Ground
25	Ground	Ground	Ground
26		Ground	Ground
27		Ground	Ground
28		Ground	Ground
29		Ground	Ground
30		Ground	Ground
31		INIT	Ground
32		FALULT	Ground
33		Not Defined	Ground
34		Not Defined	Ground
35		Not Defined	Ground
36		Selectin	Peripheral Logic High

Table 2

When connecting a 1284-A host to a 1284-B peripheral the “Peripheral Logic High” signal is not used. Similarly, when a 1284-A host is connected to a 1284-C peripheral the “Peripheral Logic High” and “Host Logic High” are not used. These two signals are optionally used to detect a “Power Off” or “Cable Disconnect” state for host and peripheral respectively.

Figure 4 shows typical Insertion Loss graphs for the PACS1284 for Data and Strobe signals. The curves are dependent on the physical location of the filter elements with respect to the ground and V_{CC} terminals of the device. These graphs are measured in a 50 Ohm environment. The signal is introduced at the series resistor input and the output is measured at the corresponding filter capacitor. The graphs labeled A,B, and C are measured between 14 (input) and 16 (output), pin 3 (input) and 26 (output), and pin 6 (input) and 23 (output), respectively. The A graph depicts "worst case" filter performance, while C represents a "best case" situation. Graphs of all other filter elements will fall in between these two.

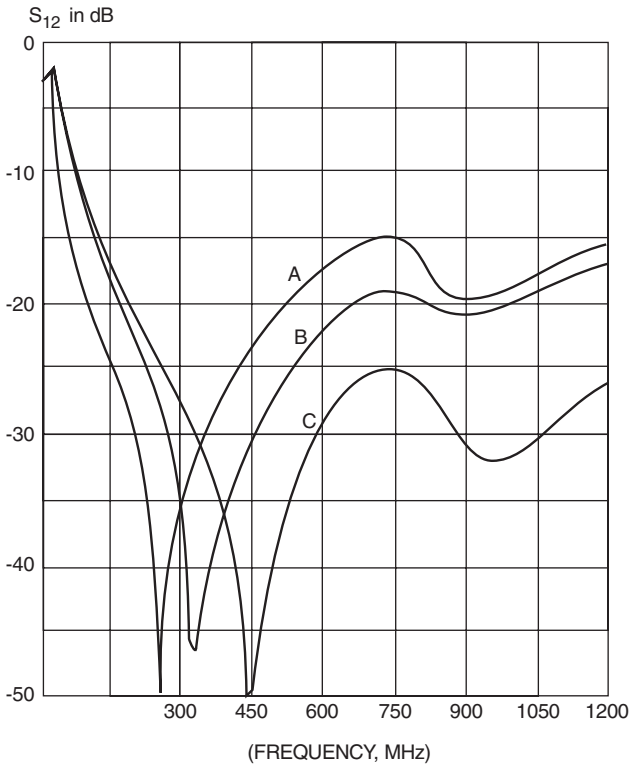


Figure 4.
Typical Filter Insertion Loss for PACS1284 (S_{12} in dB, T_A = 25° C)

Filter insertion loss is measured using Hewlett Packard HP 8753C Analyzer